WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, said method comprising:

attaching a first semiconductor chip to a first side of a printed circuit board;

attaching a second semiconductor chip to a second side of the printed circuit board opposite the first side of the printed circuit board;

using a mold to form a first mold cavity which contains the first semiconductor chip over the first side of the printed circuit board, and to form a second mold cavity which contains the second semiconductor chip over the second side of the printed circuit board; and

simultaneously filling the first and second mold cavities with a fill material via a mold inlet, wherein the mold inlet is at least partially defined through an aperture in the printed circuit board from the first side to the second side.

2. The method as claimed in claim 1, wherein the first semiconductor chip attached to the first side of the printed circuit board is aligned with the second semiconductor chip on the second side of the printed circuit board.

3. The method as claimed in claim 1, further comprising removing the mold after filling of the first and second cavities, and then separating a portion of the printed circuit board containing the aperture from a portion of the printed circuit board containing the first and second semiconductor chips.

4. The method as claimed in claim 1, wherein the mold inlet extends from a first edge of the printed circuit board to the aperture in the printed circuit board, and further from the aperture to the first and second mold cavities.

5. The method as claimed in claim 4, wherein a second edge of the printed circuit board, opposite the first edge, includes an edge connector.

6. The method as claimed in claim 1, wherein the fill material is an epoxy mold compound.

7. The method as claimed in claim 1, wherein the first and second semiconductor chips are wafer level packages.

8. A method of manufacturing a semiconductor device, said method comprising:

attaching a first semiconductor chip to a first side of a non-disposable portion of printed circuit board;

attaching a second semiconductor chip to a second side of the non-disposable portion of the printed circuit board opposite the first side of the printed circuit board;

using a mold to form a first mold cavity which contains the first semiconductor chip over the first side of the printed circuit board, and to form a second mold cavity which contains the second semiconductor chip over the second side of the printed circuit board, wherein the mold further forms a mold inlet which traverses a boundary between a disposable region and the non-disposable region of the printed circuit board;

simultaneously filling the first and second mold cavities with a fill material via the mold inlet;

removing the mold to expose the fill material defined by the first and second cavities and further defined by the mold inlet; and

separating the disposable region of the printed circuit board from the non-disposable region of the printed circuit board.

9. The method as claimed in claim 8, wherein the first semiconductor chip attached to the first side of the printed circuit board is aligned with the second semiconductor chip on the second side of the printed circuit board.

10. The method as claimed in claim 8, wherein the mold inlet extends from a first edge of the printed circuit board to the non-disposable portion of the printed circuit board.

11. The method as claimed in claim 10, wherein a second edge of the printed circuit board, opposite the first edge, includes an edge connector.

12. The method as claimed in claim 8, wherein the first and second semiconductor chips are wafer level packages.

13. A method of manufacturing a semiconductor device, said method comprising:

attaching a semiconductor chip to a first side of a non-disposable portion of printed circuit board;

using a mold to form a mold cavity which contains the semiconductor chip over the first side of the printed

circuit board, wherein the mold further forms a mold inlet which traverses a boundary between a disposable region and the non-disposable region of the printed circuit board;

filling the mold cavity with a fill material via the mold inlet;

removing the mold to expose the fill material defined by the mold cavity and further defined by the mold inlet; and

separating the disposable region of the printed circuit board from the non-disposable region of the printed circuit board.

14. The method as claimed in claim 13, wherein the mold inlet extends from a first edge of the printed circuit board to the non-disposable portion of the printed circuit board.

15. The method as claimed in claim 14, wherein a second edge of the printed circuit board, opposite the first edge, includes an edge connector.

16. The method as claimed in claim 13, wherein the semiconductor chip is a wafer level package.

17. A method of manufacturing a semiconductor device, said method comprising:

attaching a plurality of first semiconductor chips to a first side of a printed circuit board;

attaching a plurality of second semiconductor chips to a second side of the printed circuit board opposite the first side of the printed circuit board;

using a mold to form at least one first mold cavity which contains the first semiconductor chips over the first side of the printed circuit board, and to form at least one second mold cavity which contains the second semiconductor chips over the second side of the printed circuit board; and

simultaneously filling the first and second mold cavities with a fill material via at least one mold inlet.

18. The method as claimed in claim 17, wherein the mold inlet is at least partially defined by at least one aperture through the printed circuit board from the first side to the second side.

19. The method as claimed in claim 17, wherein the first plurality of semiconductor chips attached to the first side of the printed circuit board are respectively

aligned with the second plurality of semiconductor chips on the second side of the printed circuit board.

20. The method as claimed in claim 17, wherein the at least one first mold cavity includes a plurality of first mold cavities which respectively contain the plurality of first semiconductor chips, and wherein the at least one second mold cavity includes a plurality of second mold cavities which respectively contain the plurality of second semiconductor chips.

21. The method as claimed in claim 20, wherein the at least one mold inlet includes a plurality of mold inlets in fluid communication with the pluralities of first and second mold cavities, respectively.

22. The method as claimed in claim 21, wherein the plurality of mold inlets are at least partially defined by a plurality of respective apertures which extend through the printed circuit board from the first side to the second side.

23. The method as claimed in claim 22, wherein the plurality of mold inlets extend from a first edge of the printed circuit board to the respective plurality of

apertures in the printed circuit board, and further from the respective plurality of apertures to the respective pluralities of first and second mold cavities.

24. The method as claimed in claim 23, wherein a second edge of the printed circuit board, opposite the first edge, includes an edge connector.

25. The method as claimed in claim 24, further comprising removing the mold after filling of the pluralities of first and second cavities, and then separating a portion of the printed circuit board containing the plurality of apertures from a portion of the printed circuit board containing the pluralities of first and second semiconductor chips.

26. The method as claimed in claim 17, wherein the first and second semiconductor chips are wafer level packages.

27. The method as claimed in claim 19, wherein the mold inlet is at least partially defined by a plurality of apertures through the printed circuit board from the first side to the second side, and wherein the plurality of mold inlet apertures are provided in one-to-one

correspondence with the aligned first and second semiconductor packages.

28. The method as claimed in claim 19, wherein the mold inlet is at least partially defined by a plurality of apertures through the printed circuit board from the first side to the second side, and wherein the plurality of mold inlet apertures are provided in a less than one-to-one correspondence with the aligned first and second semiconductor packages.

29. The printed circuit board as claimed in claim 17, wherein the mold inlet is at least partially defined by a plurality of apertures through the printed circuit board from the first side to the second side, wherein some of the plurality of apertures are located in a disposable portion of the board body, and others of the plurality of apertures are located in a non-disposable portion of the board body, and wherein the first and second semiconductor packages are attached in the non-disposable portion of the board body.

30. The printed circuit board as claimed in claim 17, wherein thickness, length and width dimensions of the

printed circuit board are in conformance with a Joint Electronic Device Engineering Council (JEDEC) standard.

31. A method of manufacturing a semiconductor device, said method comprising:

attaching a plurality of first semiconductor chips to a first side of a non-disposable portion of printed circuit board;

attaching a plurality of second semiconductor chips to a second side of the non-disposable portion of the printed circuit board opposite the first side of the printed circuit board;

using a mold to form at least one first mold cavity which contains the first semiconductor chips over the first side of the printed circuit board, and to form at least one second mold cavity which contains the second semiconductor chips over the second side of the printed circuit board, wherein the mold further forms at least one mold inlet which traverses a boundary between a disposable region and the non-disposable region of the printed circuit board;

simultaneously filling the first and second mold cavities with a fill material via the mold inlet;

removing the mold to expose the fill material defined by the first and second cavities and further defined by the mold inlet; and

separating the disposable region of the printed circuit board from the non-disposable region of the printed circuit board.

32. The method as claimed in claim 31, wherein the first plurality of semiconductor chips attached to the first side of the printed circuit board are aligned with the second plurality of semiconductor chips on the second side of the printed circuit board.

33. The method as claimed in claim 31, wherein the mold inlet extends from a first edge of the printed circuit board to the non-disposable portion of the printed circuit board.

34. The method as claimed in claim 33, wherein a second edge of the printed circuit board, opposite the first edge, includes an edge connector.

35. The method as claimed in claim 31, wherein the first and second semiconductor chips are wafer level packages.

36. The method as claimed in claim 32, wherein the mold inlet is at least partially defined by a plurality of apertures through the printed circuit board from the first side to the second side, and wherein the plurality of mold inlet apertures are provided in one-to-one correspondence with the aligned first and second semiconductor packages.

37. The method as claimed in claim 32, wherein the mold inlet is at least partially defined by a plurality of apertures through the printed circuit board from the first side to the second side, and wherein the plurality of mold inlet apertures are provided in a less than one-to-one correspondence with the aligned first and second semiconductor packages.

38. The printed circuit board as claimed in claim 31, wherein the mold inlet is at least partially defined by a plurality of apertures through the printed circuit board from the first side to the second side, wherein some of the plurality of apertures are located in the disposable portion of the board body, and others of the plurality of apertures are located in the non-disposable portion of the board body, and wherein the first and

second semiconductor packages are attached in the non-disposable portion of the board body.

39. The printed circuit board as claimed in claim 31, wherein thickness, length and width dimensions of the printed circuit body are in conformance with a Joint Electronic Device Engineering Council (JEDEC) standard.

40. A method of manufacturing a semiconductor device, said method comprising:

attaching a plurality of semiconductor chips to a first side of a non-disposable portion of printed circuit board;

using a mold to form at least one first mold cavity which contains the semiconductor chips over the first side of the printed circuit board, wherein the mold further forms at least one mold inlet which traverses a boundary between a disposable region and the non-disposable region of the printed circuit board;

filling the at least one mold cavity with a fill material via the mold inlet;

removing the mold to expose the fill material defined by the at least one mold cavity and further defined by the mold inlet; and

separating the disposable region of the printed circuit board from the non-disposable region of the printed circuit board.

41. The method as claimed in claim 40, wherein the at least one mold inlet includes a plurality of mold inlets extending from a first edge of the printed circuit board to the non-disposable portion of the printed circuit board.

42. The method as claimed in claim 41, wherein a second edge of the printed circuit board, opposite the first edge, includes an edge connector.

43. The method as claimed in claim 40, wherein the plurality of semiconductor chips are wafer level packages.

44. A method of manufacturing a semiconductor device, comprising:

providing an elongate printed circuit board having an edge connector located on a first long edge thereof;

attaching a plurality of first wafer level packages on a first surface of the printed circuit board, the first wafer level packages attached so as to be juxtaposed along the length of the printed circuit board

between the first long edge and a second long edge of the printed circuit board;

attaching a plurality of second wafer level packages on a second surface of the printed circuit board opposite the first surface, the second wafer level packages attached so as to be juxtaposed along the length of the printed circuit board and aligned with the first wafer level packages, respectively;

using a mold to form at least one first mold cavity which contains the first wafer level packages over the first side of the printed circuit board, and to form at least one second mold cavity which contains the second wafer level packages over the second side of the printed circuit board;

simultaneously filling the first and second mold cavities with a fill material via at least one mold inlet which extends from the second edge of the printed circuit board to the first and second mold cavities.

45. The method as claimed in claim 44, wherein the at least one first mold cavity includes a plurality of first mold cavities which respectively contain the plurality of first wafer level packages, and wherein the at least one second mold cavity includes a plurality of

second mold cavities which respectively contain the plurality of second wafer level packages.

46. The method as claimed in claim 45, wherein the at least one mold inlet includes a plurality of mold inlets extending between the second edge of the printed circuit board and the pluralities of first and second mold cavities, respectively.

47. The method as claimed in claim 46, wherein a plurality of apertures extending through the printed circuit board which partially define the plurality of mold inlets, respectively.

48. A method of manufacturing a semiconductor device, said method comprising:

providing a printed circuit board having a first side and a second side opposite the first side;

attaching a semiconductor chip to the first side of the printed circuit board;

using a mold to form a first mold cavity which contains the semiconductor chip over the first side of the printed circuit board; and

filling the first mold cavity with a fill material via a mold inlet, wherein the mold inlet is at least

partially defined through an aperture in the printed circuit board from the first side to an opposite second side, wherein the aperture is located outside of a portion of the printed circuit board underlying the attached semiconductor chip.

49. The method as claimed in claim 48, wherein the first semiconductor chip is a wafer level package.

50. The method as claimed in claim 48, wherein the aperture is located in a disposable portion of the printed circuit board, and wherein the method further comprises separating the disposable portion of the printed circuit board from a remaining portion of the printed circuit board which contains the semiconductor chip.

51. A printed circuit board comprising:

a flat, elongate board body having a first surface and an opposite second surface, and further having a first long edge and an opposite second long edge;

an edge connector located on said first long edge of said board body;

a first plurality of semiconductor package mounting regions on the first surface of the board body and

juxtaposed along the length of the board body between the first long edge and a second long edge;

a second plurality of semiconductor package mounting regions on the second surface of said board body and respectively aligned with the first plurality of wafer level package mounting regions; and

a plurality of mold inlet apertures extending through said board body and located between second long edge and said semiconductor package mounting regions.

52. The printed circuit board as claimed in claim 51, wherein the plurality of mold inlet apertures are provided in one-to-one correspondence with the aligned first and second semiconductor package mounting regions.

53. The printed circuit board as claimed in claim 51, wherein the plurality of mold inlet apertures are provided in a less than one-to-one correspondence with the aligned first and second semiconductor package mounting regions.

54. The printed circuit board as claimed in claim 51, wherein the plurality of mold inlet apertures are located in a disposable portion of the board body, and the first and second semiconductor package mounting

regions are located in a non-disposable portion of the board body.

55. The printed circuit board as claimed in claim 51, wherein some of the plurality of mold inlet apertures are located in a disposable portion of the board body, and others of the plurality of mold inlet apertures are located in a non-disposable portion of the board body, and wherein the first and second semiconductor package mounting regions are located in a non-disposable portion of the board body.

56. The printed circuit board as claimed in claim 51, wherein thickness, length and width dimensions of the board body are in conformance with a Joint Electronic Device Engineering Council (JEDEC) standard.

57. The printed circuit board as claimed in claim 54, wherein thickness, length and width dimensions of the non-disposable portion of the board body are in conformance with a Joint Electronic Device Engineering Council (JEDEC) standard.

58. The printed circuit board as claimed in claim 55, wherein thickness, length and width dimensions of the

non-disposable portion of the board body are in conformance with a Joint Electronic Device Engineering Council (JEDEC) standard.

59. The printed circuit board as claimed in claim 51, wherein the first and second semiconductor packages are wafer level packages.

60. The printed circuit board as claimed in claim 54, wherein the first and second semiconductor packages are wafer level packages.

61. The printed circuit board as claimed in claim 55, wherein the first and second semiconductor packages are wafer level packages.